TECHNICAL ARTICLE

Passing EMI Compliance Testing the First Time—Part 2: PCB Radiation Examples

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Abstract

Any product designed today that requires high speed clocks can be troubled with electromagnetic compatibility (EMC) compliance issues. This article outlines an electromagnetic (EM) field-oriented perspective for printed circuit board (PCB) design intended to help the reader pass electromagnetic interference (EMI) testing the first time. The same techniques used for reducing EMI will mitigate interference, suggesting a universal PCB layout philosophy. This article is presented in three sections. This second article covers several PCB interconnect examples illustrating exactly how to implement the techniques presented in Part 1. Finally, Part 3 will discuss PCB layout strategies for complex boards that will satisfy the presented solutions.

Introduction

Part 1 covered all the essential physics needed to understand why we need to use transmission lines to confine field energy in our layout to manage electromagnetic interference (EMI). It ended with a short list of common printed circuit board (PCB) layout challenges that need to be addressed, repeated below.

On the PCB, field confinement is commonly lost when

1. Signals transition between layers
2. Signals share the same volume over a common ground plane
3. Signals cross one another over a shared ground plane
4. Signals are run in parallel
5. Field fringing occurs
6. Signals propagate down a microstrip or other imperfect transmission line

This second article addresses these issues with two examples representing the most common sources of PCB radiation overlooked by even experienced engineers.

The Transmission Line Can Radiate

Consider a logic gate about to raise its output voltage. Assuming that the IC's decoupling capacitor is close by, where is the stored energy that is about to be used? It is locally stored in the dielectric (the space) inside the decoupling capacitor. Now imagine the IC raising its output voltage by moving charge to the output pin previously at ground. The charge that was moved has a field that will immediately reach out at the speed of light and exert a force on any charge that it encounters. Fortunately, the ground plane will be the closest source of charge and, being a good conductor, it takes very little energy to move a canceling charge directly under the trace. The electric force ensures that this canceling charge is as close as possible to the original charge provided by the logic gate. From this point on, for distant locations outside this small dipole, the field will be nearly zero and this becomes truer the farther in time and distance a location gets from these two canceling charges. For the fields generated from the accelerating charges, there will be a displacement current in the decoupling capacitor as well as in the dielectric between the output trace and the ground plane where the voltage transition

is taking place. There are accelerating charges throughout the entirety of this electrically small loop (some provided by that changing electric field, which is a current). When the size of a current loop is small compared to the distance from which it is observed, the accelerating segments of the loop cancel each other out. As a result, the net accelerating charge appears to be zero from a distant vantage point.

The relativistic field described in Faraday's law is critical to understanding EMI. All charges possess a coulomb field but when charges are moving (relatively speaking) and accelerating, there are two additional electric fields that contribute to the total electric field. Motion and acceleration twist the coulomb field to be the sum of three components. When charges move relative to others, special relativity compresses space just enough so that normally electrically neutral circuits develop a net charge. Mathematically, this is called magnetism, but a real electric field is developed due to this relative motion. The third and last electric field is caused from the acceleration of charges and is directed transverse to the original acceleration (but opposite direction). The energy contained within these two additional fields is different from what is stored in the coulomb field. Both the magnetic field as well as the transverse E field are relativistic. This means that the stored energy involved can be situational. It is only real from a dimensionally orthogonal perspective, and this has the interesting consequence of removing a coordinate of space. Where the coulomb field energy is stored in three dimensions of space, this transverse field's energy is present and stored in two dimensions of space. For Faraday's law, this means that the line integral of E around any closed path will be nonzero when this transverse field is present (when charges are accelerating). It also means that the energy attenuates less aggressively with distance than the coulomb field, spreading with the surface area rather than the volume.

The transverse field from the accelerating charge will create an opposing field that will also act on charges in the ground plane. The charges in the ground plane move based on the superposition of all three electric forces, and the net effect causes the canceling current to move from the required direction to eliminate the changing magnetic field of the original accelerating charge. Armed with this knowledge, we can predict exactly what will happen as the leading edge of a signal propagates down a transmission line. The decoupling capacitor, as well as the transmission line before the propagating leading edge, will see a fixed forward and return current as the displacement current moves down the line. Only the displacement current at the leading edge of the wave will radiate as this very tiny electrically small segment with a length equal to the distance between the signal trace and the ground plane travels down the transmission line. There is no close return current for this segment of displacement current so its field will spread out causing radiation and EMI. As mentioned earlier, the length of the transmission line both before and after the leading edge will remain electrically quiet. This displacement current at the location where the voltage is in transition on the transmission line is an often-overlooked normal source of radiation. This very tiny segment of accelerating charge may not look significant, but there are thousands of these transmission lines running on a complex board all on a common clock. Generally, common clock sources of radiation sum in a complex way at the network analyzer. This could represent a significant source of radiation due to the superposition of energy.

The Resonant Circuit

In addition to imperfect transmission lines, the average PCB is also packed with resonant circuits. These are all the necessary analog connections required, including op amp input/output nets, switching power supply interconnects, measurement pathways, and more. The trouble is that they don't stand out as different from the transmission lines to most designers. We can turn the properly terminated transmission line above into a resonant circuit by terminating the line into a capacitor (or a short) instead of a resistor. After this simple change, the entire circuit is now only composed of reactive elements—namely, the L and C from the transmission line and the capacitive or inductive terminations. If the line is long enough or the capacitive termination large enough, this circuit can resonate low enough to affect emissions. This is especially true if the current in the line is high. Higher currents always result in more radiation.

For a properly terminated transmission line, energy moves down line only once for each edge. Even for long lines at 0.66 C, that little radiation segment is not around for long even for very long PCB traces. See Figure 1. In contrast, the resonant circuit doesn't have any resistance to dissipate energy so a single step input will cause the line to resonate at $1/2\pi\sqrt{LC}$ until the energy is radiated away.

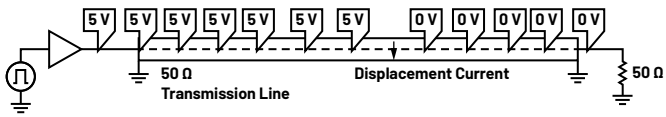

Figure 1. For a properly terminated transmission line, radiation will occur where the signal is transitioning due to the displacement current of the changing electric field.

The most troublesome resonant circuit of all is the hot loop on a switching power supply. Figure 2 shows two switching power supply layouts. Most engineers would consider the second to be a good layout but it is not. The hot loop is a high Q resonant circuit composed of some low resistance interconnects terminated on one end to a very low impedance (high capacitance) supply, while the other end connects to the buck MOSFETs as shown. The simplified circuit and the simulation are shown in Figure 3. Although it may not seem that a few nanohenries and the 400 pF of the lower MOSFET Cds would resonate well within the CISPR class B frequency range, but they do. This circuit is the perfect storm for noise:

- The resonant circuit lies within the EMI compliance region.
- It is a series resonant circuit that will short at resonance (maximizing the current), and it is driven with a low inductance voltage source.

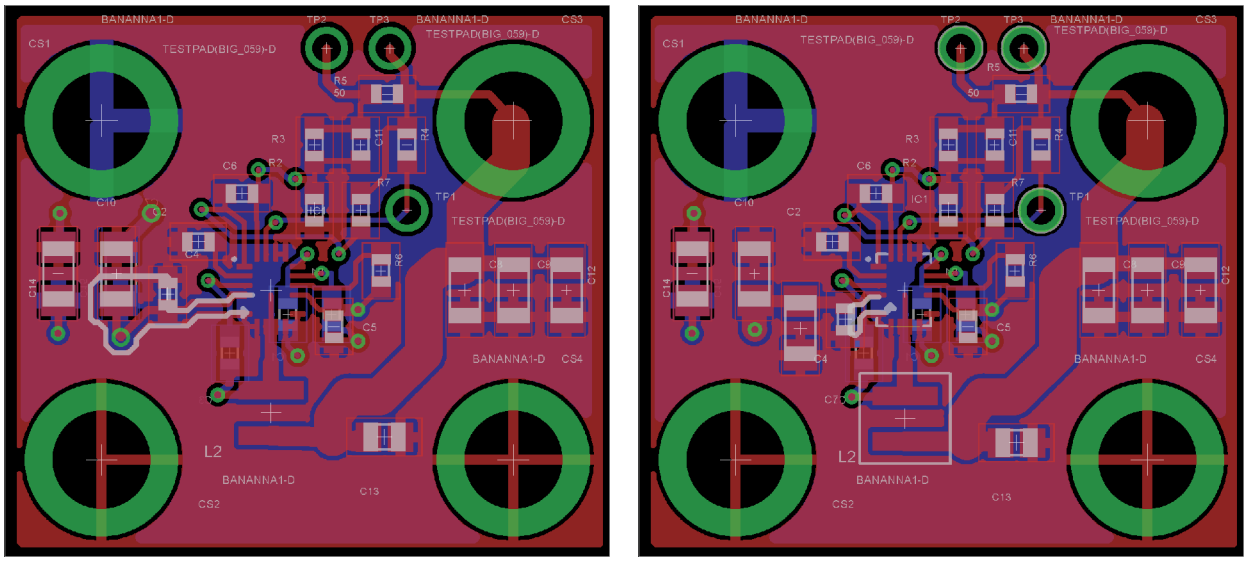

Figure 2. The left image shows an incorrect hot loop layout for an LT8641A. The highlighted loop will easily resonate under 1 GHz. The right image is an example of a good switching power supply hot loop layout.

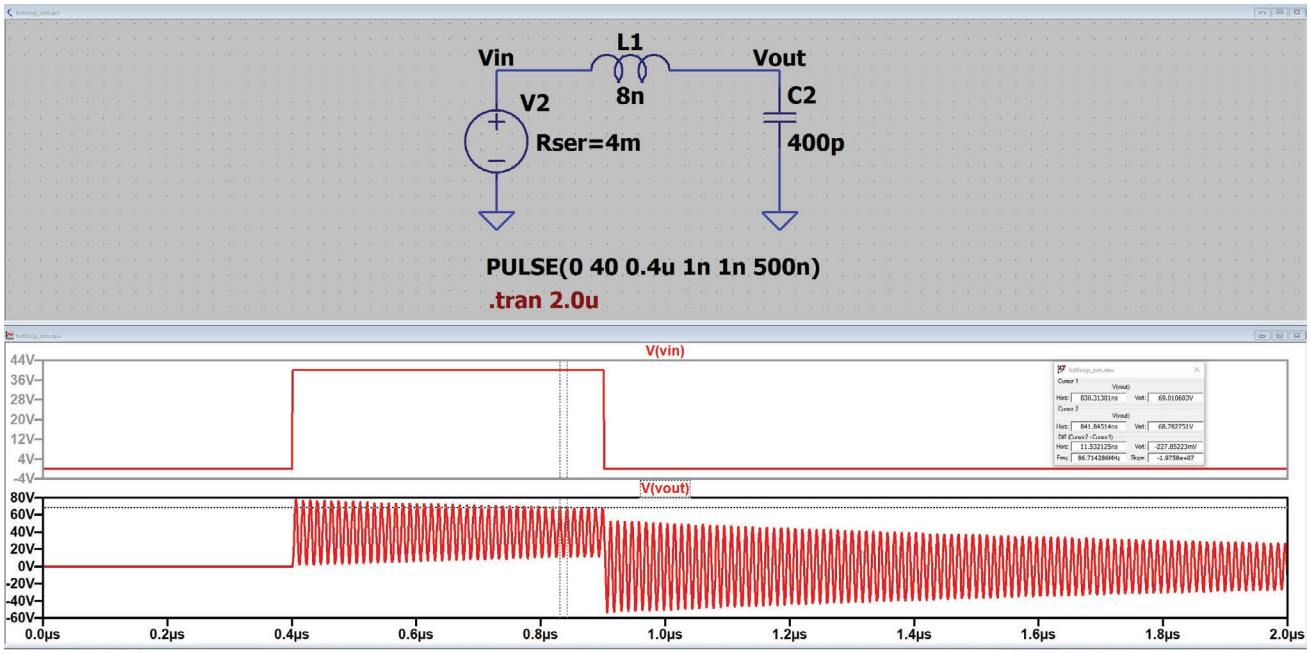

Figure 3. The simulation above shows the importance of managing the hot loop inductance. Note that an 8 nH hot loop can resonate at 88 MHz. Radiation from this loop can be significant even though the loop is electrically small (due to the high currents).

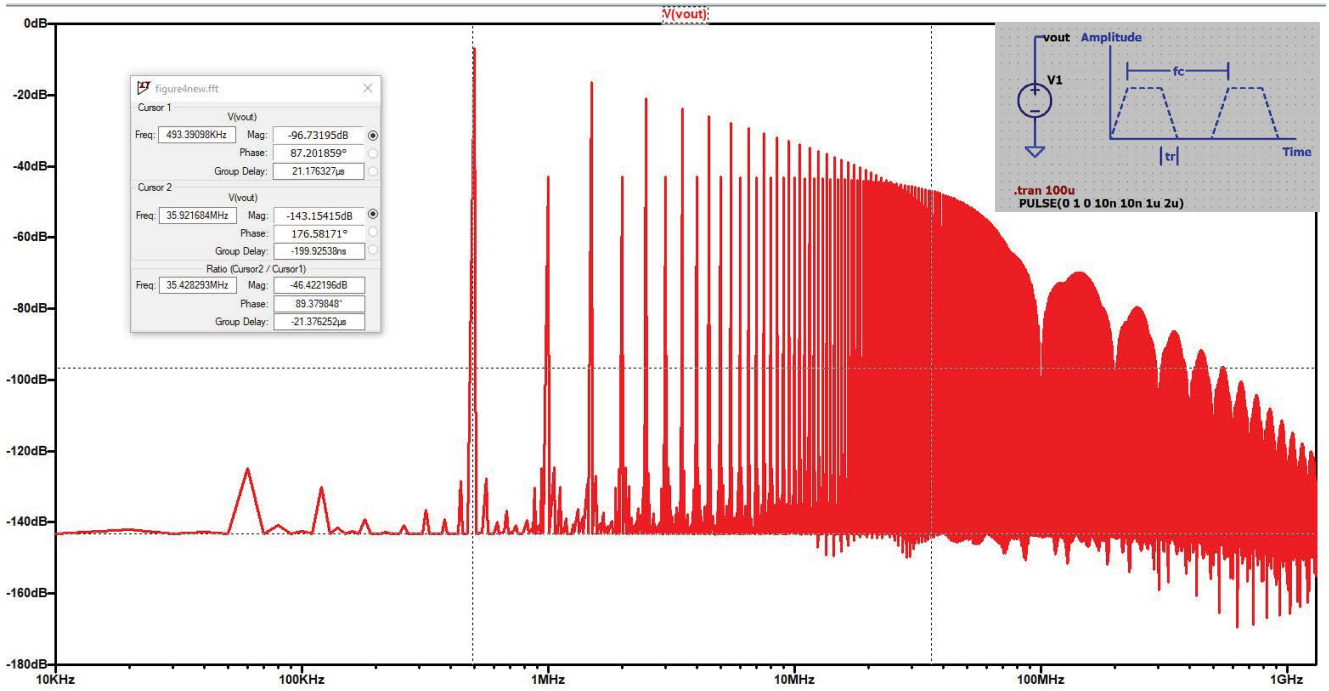

Figure 4. The Fourier analysis of an imperfect square wave contains energy at each odd harmonics. This realistic waveform also has two infection points. One at f = 2 fc/(π)(20 dB/dec), and a second at 1/(π)tr(40 dB/dec).

- It is driven with a high voltage square wave with significant harmonic content reasonably close to the resonant frequency. There is always harmonic content near the resonant frequency.
- Since the circuit is high Q (very low real resistance), the energy continues to move back and forth between the inductor to the capacitor and back until all the energy is radiated away.
- The slow very high capacitance (higher than Cds) body diode of the synchronous MOSFET maximizes the initial current when the switch turns on. For example, for a buck converter with V_{IN} = 48 V, the body diode could experience 48 V over as little as 1 ns. For Cds = 400 pF (discounting the inductance and the reverse recovery charge in the conducting body diode of the synchronous switch), the initial current would then be I = Cdv/dt or ~20 A. This current is only limited by L.

Since the initial current is so high, there ends up being significant energy at the harmonics near the circuit resonant frequency. This is why emission failures can be seen just about anywhere from the same buck controller operating at the same frequency for different designs. The emission location is all about where that series LC resonant circuit is shorting, and how much harmonic current content is present. Reducing the current at the fundamental (lowering the voltage) or reducing the switch-mode power supply (SMPS) fundamental frequency (running the converter at a lower frequency) helps, since that will attenuate the offending harmonic. Lowering the slew rate to something below the resonant frequency will also improve matters. See Figure 3. To avoid this issue, the frequency of this resonant circuit can be increased (this is how the hot loop should be eliminated). At the higher resonant frequency there will be much lower harmonic content (see Figure 4) and smaller inductors and capacitors will store less energy.

The same issue exists in the gate turn on circuit to a much smaller degree. In this circuit, 10 Ω of gate resistance can be added to dampen the circuit and components can be placed much closer lowering the inductance, resulting in a better damped higher resonant frequency loop.

It's important to note that the DC power system on the board needs to be constructed with low impedance transmission lines. With the transmission line impedance equal to $\sqrt{(L/C)}$, a low characteristic impedance implies small L and high C, which is constructed with a small space between the supply track and the ground return. This geometry provides a larger energy pipe for all the circuits receiving power. Since the conductors are very close, the structure will provide a very low external magnetic field, and the confined magnetic field will be much higher since all the magnetic field needs to exist in a smaller volume. With the electric field also high due to the thin dielectric, the power flow, P = ExH, as described by Poynting's vector, will also be large. Improving upon this can be accomplished only by reducing the board impedance with multiple layer pairs of supply and ground plane since there are limitations in the PCB construction process. Note that higher characteristic impedance lines can still move large amounts of energy. However, more area is required to make this happen since the same voltage and current levels will result in smaller E and H fields in the dielectric. The larger inductance will take more time to change the stored energy (the higher load current) while the line voltage on the capacitance did not change at all for this fixed supply. All this means is that the lower inductance line is more flexible when it comes to changing the power flow quickly.

Looking back at that list of common PCB layout challenges shared in the introduction, it's easy to see how these imperfections can

be inadvertently introduced in the examples above. In layout it is common to break the transmission line momentarily by changing layers. This layer change can easily introduce a length of transmission line (the via distance) that will not have a close return current unless a ground stitching via is placed adjacent. With multilayer boards, the design may be compromised by serving more than one signal layer to a single ground plane. In a compact board, traces may be run in parallel over long distances over a common ground plane. Either of these practices will allow fields from different signals to mix causing interference. Finally, much like the via described above, the microstrip transmission line does not quarantine the magnetic field at the leading edge of the signal propagation. This energy is free to radiate in the plane of the board.

In Part 3, PCB layout strategies will be discussed to help design out as many of these imperfections as possible. In addition, a third example (power delivery) will be added to the two examples presented in this article.

Conclusion

The first article in the series presented the field-oriented view of layout and covered the fundamental physics supporting the presented layout strategy. This second article illustrated how a short list of common layout practices can compromise EMI and generate interference using just two PCB interconnection examples, the transmission line and the resonant circuit. An imperfect layout can cause interference and EMI from either of these sources even if circuit currents are low depending on the location of the victim circuit, how many transmission lines are involved, and the magnitude of the circuit currents (such as a hot loop within an SMPS). The techniques used to manage EMI and interference will also improve the PCB susceptibility to externally generated fields. Finally, how the commonly used resonant circuit, being composed of only reactive components will resonate, exploits the imperfections discussed to radiate energy.

The next article in the series will introduce a final circuit type (power delivery) and present a PCB layout strategy covering both power and signal delivery for a complex PCB.

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