

Generating MIPI C-PHY and D-PHY Compatible Waveforms with ADATE334, a 2.3GHz High-Speed Dual Integrated DCL

**INTRODUCTION**

The ADATE334 is a complete dual-channel automatic test equipment (ATE) solution that performs the pin electronics functions of driver, comparator, and active load (DCL), and four-quadrant per pin parametric measurement unit (PPMU). Dedicated 16-bit DACs with on-chip calibration registers provide all necessary DC levels for operation of the device.

The high voltage driver features three active states: high (VIH), low (VIL), and terminate mode (VIT), as well as a high impedance inhibit state (HiZ). The inhibit state, in conjunction with the integrated dynamic clamps, facilitates significant attenuation of transmission line reflections when the driver is not actively terminating the line.

The open circuit drive capability is  $-1.5V$  to  $+7.0V$  to accommodate a wide range of ATE and instrumentation applications. The low voltage driver, working in conjunction with the high voltage driver, can provide 25mVpp to 600mVpp signals at up to 4.6Gbps in a 50Ω environment. Refer to the [ADATE334](#) data sheet and functional block diagram for more information.

The MIPI Alliance provides a set of specialized physical layers with both complementary and unique features. MIPI C-PHY and MIPI D-PHY are mainly used for camera, display, and mobile applications. The ADATE334 high voltage and low voltage drivers can be used in combination to generate multilevel waveforms that are MIPI C-PHY and D-PHY compatible.

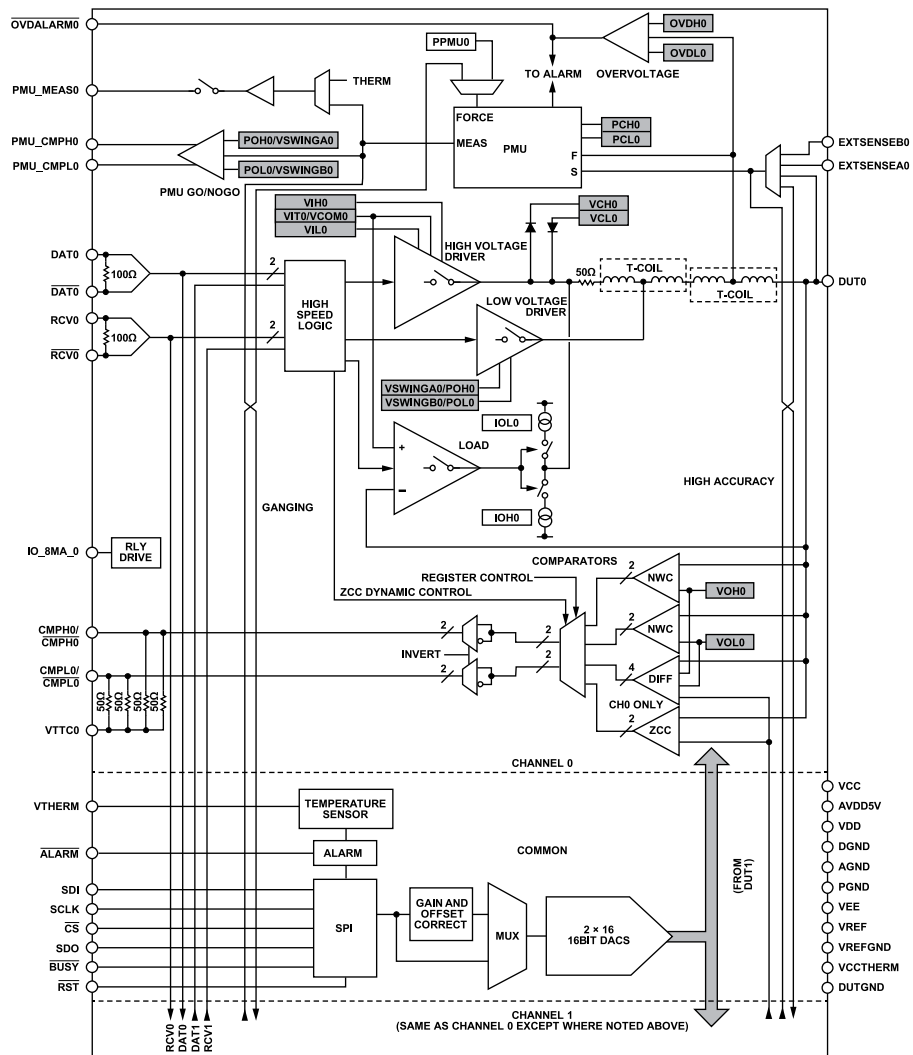


Figure 1. ADATE334 Functional Block Diagram

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**REVISION HISTORY****7/2025—Revision 0: Initial Version**

### ADATE334 HIGH-SPEED MUX AND DRIVER CONTROLS

The ADATE334 utilizes internal high-speed multiplexers to map the high-speed inputs (DAT0, RCV0, DAT1, and RCV1) to the internal high voltage or low voltage driver control signals. The block diagram in Figure 1 shows the arrangement of the internal multiplexers and output drivers. The internal multiplexers (HV\_DAT\_x, HV\_RCV\_x, LV\_VSWA\_x, and LV\_VSWB\_x) generate the internal high-speed high voltage driver control signals (SELECTED\_DAT\_x and SELECTED\_RCV\_x) and low voltage driver control signals (SELECTED\_VSWA\_x and SELECTED\_VSWB\_x). Table 1 shows how the high voltage driver control signals determine the state of

the high voltage driver output and Table 2 shows how the low voltage driver control signals determine the state of the low voltage driver output. The ADATE334 output is the sum of the high voltage driver and low voltage driver outputs.

The internal multiplexer selection is controlled via Register 0x05 and is described in Table 3 to Table 6. Utilizing these internal multiplexers, different combinations of high voltage and low voltage driver outputs can be created using the high-speed inputs.

Table 1. Internal High Voltage Driver Control Truth Table

SELECTED_RCV_X	SELECTED_DAT_X	High Voltage Driver Output
0	0	VIL
0	1	VIH
1	0	VIT
1	1	VIT

Table 2. Internal Low Voltage Driver Control Truth Table

SELECTED_VSWB_X	SELECTED_VSWA_X	Low Voltage Driver Output
0	0	$-\frac{1}{2} VSWA - \frac{1}{2} VSWB$
0	1	$-\frac{1}{2} VSWB$
1	0	$-\frac{1}{2} VSWA$
1	1	-0(OFF)

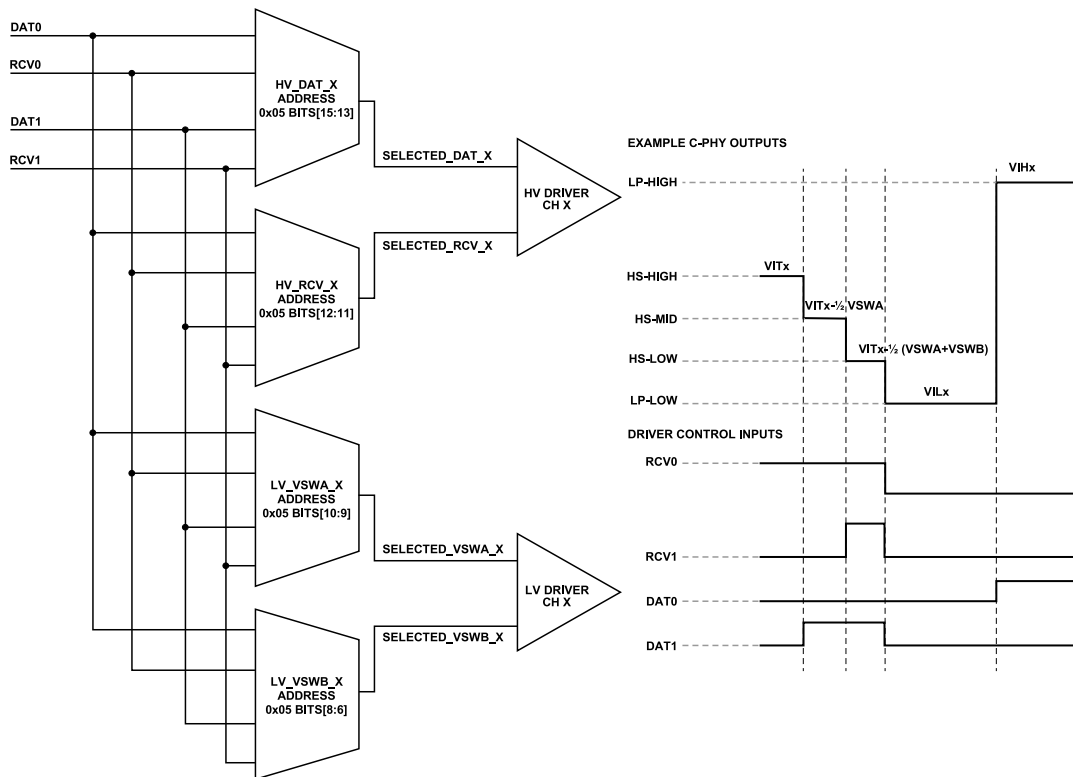


Figure 2. ADATE334 High-Speed Multiplexer to Driver Input Selection Diagram and Example C-PHY Outputs

## HIGH-SPEED MULTIPLEXERS TO DRIVER INPUT SELECTION

Table 3. Map HV\_DAT\_X to High Voltage Driver Input

HV_DAT_0[2:0] Address 0x05[15:13]	SELECTED_DAT_0	HV_DAT_1[2:0] Address 0x05[15:13]	SELECTED_DAT_1
000	DAT0	000	DAT1
001	DAT1	001	DAT0
010	DAT1	010	DAT0
011	Reserved	011	Reserved
100	Reserved	100	Reserved
101	Reserved	101	Reserved
110	Reserved	110	Reserved
111	High	111	High

Table 4. Map HV\_RCV\_X to High Voltage Driver Input

HV_RCV_0[1:0] Address 0x05[12:11]	SELECTED_RCV_0	HV_RCV_1[1:0] Address 0x05[12:11]	SELECTED_RCV_1
00	RCV0	00	RCV1
01	RCV1	01	RCV0
10	RCV1	10	RCV0
11	Low	11	Low

Table 5. Map LV\_VSWA\_X to Low Voltage Driver Input

LV_VSWA_0[1:0] Address 0x05[10:9]	SELECTED_VSWA_0	LV_VSWA_1[1:0] Address 0x05[10:9]	SELECTED_VSWA_1
00	DAT0	00	DAT1
01	DAT1	01	DAT0
10	Reserved	10	Reserved
11	High	11	High

Table 6. Map LV\_VSWB\_X to Low Voltage Driver Input

LV_VSWB_0[2:0] Address 0x05[8:6]	SELECTED_VSWB_0	LV_VSWB_1[2:0] Address 0x05[8:6]	SELECTED_VSWB_1
000	DAT0	000	DAT1
001	DAT1	001	DAT0
010	RCV0	010	RCV1
011	RCV1	011	RCV0
100	Reserved	100	Reserved
101	Reserved	101	Reserved
110	Reserved	110	Reserved
111	High	111	High

## MIPI ALLIANCE

MIPI Alliance supports a wide variety of application protocols requiring high performance, low-power serial interfaces. The MIPI C-PHY and D-PHY specifications are primarily used for the connection of cameras and display applications to a host processor. The PHY functionality includes a high-speed (HS) mode for fast-data traffic and a low-power (LP) mode for control purposes. C-PHY utilizes

five signaling levels (LP-LOW, LP-HIGH, HS-LOW, HS-MID, and HS-HIGH), which can be combined across three lanes to generate the states described in Table 7. D-PHY utilizes four signaling levels (LP-LOW, LP-HIGH, HS-LOW, and HS-HIGH), which can be combined across two lanes to generate the states described in Table 8.

**Table 7. C-PHY Lane State Descriptions**

State Code	Line Voltage Levels			High-Speed	Low-Power	
	A Line	B Line	C Line	Burst Mode	Control Mode	Escape Mode
HS_+X	HS-HIGH	HS-LOW	HS-MID	+x state	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
HS_-X	HS-LOW	HS-HIGH	HS-MID	-x state	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
HS_+Y	HS-MID	HS-HIGH	HS-LOW	+y state	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
HS_-Y	HS-MID	HS-LOW	HS-HIGH	-y state	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
HS_+Z	HS-LOW	HS-MID	HS-HIGH	+z state	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
HS_-Z	HS-HIGH	HS-MID	HS-LOW	-z state	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
LP-000	LP-LOW	LP-LOW	LP-LOW	N/A <sup>1</sup>	Bridge	Space
LP-001	LP-LOW	LP-LOW	LP-HIGH	N/A <sup>1</sup>	HS-Rqst	Mark-0
LP-100	LP-HIGH	LP-LOW	LP-LOW	N/A <sup>1</sup>	LP-Rqst	Mark-1
LP-111	LP-HIGH	LP-HIGH	LP-HIGH	N/A <sup>1</sup>	Stop	N/A <sup>1,3</sup>

<sup>1</sup> N/A means not applicable.

<sup>2</sup> During high-speed transmission, the low-power receivers observe LP-000 on the lines.

<sup>3</sup> If LP-111 occurs during escape mode, the lane returns to stop state (control mode LP-111).

**Table 8. D-PHY Lane State Descriptions**

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS-LOW	HS-HIGH	Differential-0	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
HS-1	HS-HIGH	HS-LOW	Differential-1	N/A <sup>1,2</sup>	N/A <sup>1,2</sup>
LP-00	LP-LOW	LP-LOW	N/A <sup>1</sup>	Bridge	Space
LP-01	LP-LOW	LP-HIGH	N/A <sup>1</sup>	HS-Rqst	Mark-0
LP-10	LP-HIGH	LP-LOW	N/A <sup>1</sup>	LP-Rqst	Mark-1
LP-11	LP-HIGH	LP-HIGH	N/A <sup>1</sup>	Stop	N/A <sup>1,3</sup>

<sup>1</sup> N/A means not applicable.

<sup>2</sup> During high-speed transmission, the low-power receivers observe LP-00 on the lines.

<sup>3</sup> If LP-11 occurs during escape mode, the lane returns to stop state (control mode LP-11).

### C-PHY DRIVER EXAMPLE

The ADATE334 can be used to generate the five signaling levels utilized by C-PHY: LP-LOW, LP-HIGH, HS-LOW, HS-MID, and HS-HIGH. The HS signals have a smaller voltage swing at higher speeds and can be generated with the low voltage driver. The LP signals have a larger voltage swing at lower speeds and can be generated with the high voltage driver.

Figure 3 shows the C-PHY signaling levels and an example of corresponding ADATE334 output voltage levels. The internal high-speed multiplexers can be utilized to generate these output states

with the high-speed inputs (DAT0, RCV0, DAT1, and RCV1). Table 9 shows how to configure the relevant ADATE334 registers to achieve this example configuration. Table 11 shows the corresponding truth table, mapping the high-speed inputs states to specific high voltage driver and low voltage driver output levels. Under this configuration, RCV0 and DAT0 control the high voltage driver, and DAT1b and RCV1b control the low voltage driver. Figure 4 shows an example scope capture of the ADATE334 in this configuration.

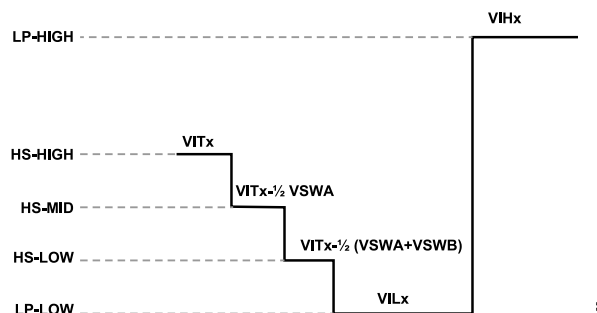


Figure 3. C-PHY Single Channel Signaling Level Example

Table 9. C-PHY Driver Mode Register Setting Example

Register Address	Name	CHx Value	CHx Mux Input
LOADCTL (0x05) [15:13]	HV_DAT_x[2:0]	000	DAT0
LOADCTL (0x05) [12:11]	HV_RCV_x[1:0]	00	RCV0
LOADCTL (0x05) [10:9]	LV_VSWA_x[1:0]	01	DAT1b
LOADCTL (0x05) [8:6]	LV_VSWB_x[2:0]	011	RCV1b
DRVCTL (0x03) [6]	DRIVE_VT_HIZ_x	1	N/A <sup>1</sup>
DRVCTL (0x03) [5:3]	DRIVE_FORCE_STATE_x[2:0]	XXX	N/A <sup>1</sup>
DRVCTL (0x03) [2]	DRIVE_FORCE_x	0	N/A <sup>1</sup>
DRVCTL (0x03) [1:0]	DRIVE_ENABLE_x[1:0]	1X	N/A <sup>1</sup>

<sup>1</sup> N/A means not applicable.

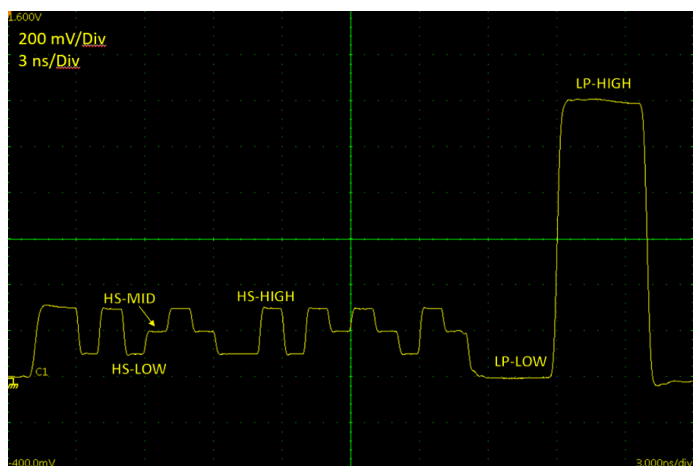


Figure 4. C-PHY Waveform Scope Picture, 1Gbps

### D-PHY DRIVER EXAMPLE

The ADATE334 can be used to generate the four signaling levels utilized by D-PHY: LP-LOW, LP-HIGH, HS-LOW, and HS-HIGH. The HS signals have a smaller voltage swing at higher speeds and can be generated with the low voltage driver. The LP signals have a larger voltage swing at lower speeds and can be generated with the high voltage driver.

Figure 5 shows the D-PHY signaling levels and an example of corresponding ADATE334 output voltage levels. The internal high-speed multiplexers can be utilized to generate these output states

with the high-speed inputs (DAT0, RCV0, DAT1, and RCV1). Table 10 shows how to configure the relevant ADATE334 registers to achieve this example configuration. Table 12 shows the corresponding truth table, mapping the high-speed inputs states to specific high voltage driver and low voltage driver output levels. Under this configuration, DAT0, DAT1, and RCV0 control the high voltage drivers, and RCV1 controls the low voltage drivers. Figure 6 shows an example scope capture of the ADATE334 in this configuration.

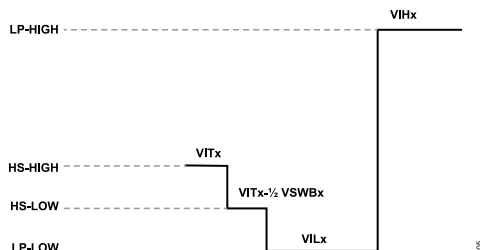


Figure 5. D-PHY Single Channel Signaling Level Example

Table 10. D-PHY Driver Mode Register Setting Example

Register Address	Name	CH0 Value	CH0 Mux Input	CH1 Value	CH1 Mux Input
LOADCTL (0x05) [15:13]	HV_DAT_x[2:0]	000	DAT0	000	DAT1
LOADCTL (0x05) [12:11]	HV_RCV_x[1:0]	10	RCV1	00	RCV1
LOADCTL (0x05) [10:9]	LV_VSWA_x[1:0]	11	High	11	High
LOADCTL (0x05) [8:6]	LV_VSWB_x[2:0]	010	RCV0	011	RCV0b
DRVCTL (0x03) [6]	DRIVE_VT_HIZ_x	1	N/A <sup>1</sup>	1	N/A <sup>1</sup>
DRVCTL (0x03) [5:3]	DRIVE_FORCE_STATE_x[2:0]	XXX	N/A <sup>1</sup>	XXX	N/A <sup>1</sup>
DRVCTL (0x03) [2]	DRIVE_FORCE_x	0	N/A <sup>1</sup>	0	N/A <sup>1</sup>
DRVCTL (0x03) [1:0]	DRIVE_ENABLE_x[1:0]	1X	N/A <sup>1</sup>	1X	N/A <sup>1</sup>

<sup>1</sup> N/A means not applicable.

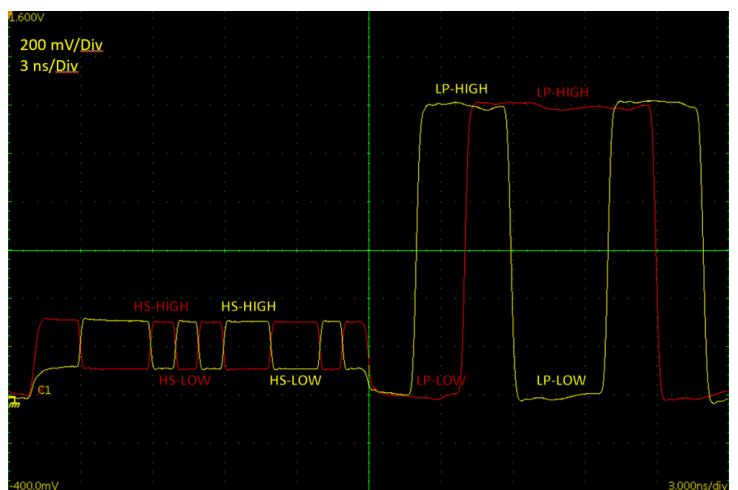


Figure 6. D-PHY Scope Plot, 1Gbps

Table 11. C-PHY Driver Mode Use Case Example

HV_DAT_0[2:0] Address		HV_RCV_0[1:0] Address		LV_SWA_0[1:0] Address		LV_SWB_0[2:0] Address		HV_DAT_1[2:0] Address		HV_RCV_1[1:0] Address		LV_SWA_1[1:0] Address		LV_SWB_1[2:0] Address		Rcv DAT0		Rcv DAT1		Low Voltage Driver State, Channel x		High Voltage Driver State, Channel x		C-PHY Lane Level
0x05[15:13]		0x05[12:11]		0x05[10:9]		0x05[8:6]		0x05[15:13]		0x05[12:11]		0x05[10:9]		0x05[8:6]		0 1		DAT0 DAT1		Channel x		Channel x		
Load Control Register, 0x05												High-Speed Inputs												
000 (DAT0)	00 (RCV0)	01 (DAT1b)	011 (RCV1b)	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	VIL	LP-LOW			
								0	0	1	0	0	0	0	0	0	0	0	0	VIH	LP-HIGH			
								1	1	X	1	- 1/2 VSWA - 1/2 VSWB	VIT	HS-LOW										
								1	0	X	1	- 1/2 VSWA	VIT	HS-MID										
								1	0	X	0	0	VIT	HS-HIGH										

Table 12. D-PHY Driver Mode Use Case Example

HV_DAT_0[2:0] Address		HV_RCV_0[1:0] Address		LV_SWA_0[1:0] Address		LV_SWB_0[2:0] Address		HV_DAT_1[2:0] Address		HV_RCV_1[1:0] Address		LV_SWA_1[1:0] Address		LV_SWB_1[2:0] Address		Rcv DAT0		Rcv DAT1		Low Voltage Driver State, Channel		High Voltage Driver State, Channel		Low Voltage Driver State, Channel	High Voltage Driver State, Channel	D-PHY State Code
0x05[15:13]		0x05[12:11]		0x05[10:9]		0x05[8:6]		0x05[15:13]		0x05[12:11]		0x05[10:9]		0x05[8:6]		0 1		DAT 0 DAT 1		Channel 0 Channel 1		Channel 1 Channel 1		Channel 1	Channel 1	
Load Control Register, 0x05												High-Speed Inputs				Dp-Line		Dn-Line								
000 (DAT0)	10 (RCV1)	11 (High)	010 (RCV0)	000 (DAT1)	00 (RCV1)	11 (High)	011 (RCV0b)	0	0	0	0	- 1/2 VSWB0	VIL0	0	VIL1	LP-00										
								0	0	1	0	- 1/2 VSWB0	VIH0	0	VIL1	LP-10										
								0	0	0	1	- 1/2 VSWB0	VIL0	0	VIH1	LP-01										
								0	0	1	1	- 1/2 VSWB0	VIH0	0	VIH1	LP-11										
								0	1	X	X	- 1/2 VSWB0	VIT0	0	VIT1	HS-0										
								1	1	X	X	0	VIT0	- 1/2 VSWB1	VIT1	HS-1										

## REFERENCES

MIPI. 2022. <https://www.mipi.org/>.

*ADATE334 Data Sheet, 2.3 GHz Dual Integrated DCL with PPMU, Level Setting DACs, and On-Chip Calibration Registers.* Analog Devices.

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