Upgrading GMSL2 to GMSL3

ABSTRACT

This article details the design considerations when upgrading an existing GMSL2™ design to a GMSL3™ design. The specific examples use a GMSL2 sensor pair, the MAX96717 and MAX96716A, and a pin-for-pin compatible GMSL3 sensor pair, the MAX96793 and MAX96792A. The article covers the benefits of GMSL3 along with design considerations for upgrading from GMSL2 to GMSL3.

INTRODUCTION

One of the primary benefits of the GMSL™ technology is the intergeneration compatibility between devices within one generation. GMSL2 is backwards compatible with GMSL1™ and GMSL3 is backwards compatible with GMSL2; verify the part's compatibility by using the data sheet. This flexibility also translates to time savings by maintaining the same pin and package to reuse designs for compatible parts.

GMSL3 OVERVIEW

The main difference with GMSL3 is doubling the GMSL data rate on the link up to 12Gbps. GMSL2 is typically sufficient for most applications, however, sensor and display bandwidths continue to increase. GMSL3 aims to achieve these higher data rates while maintaining all the benefits of GMSL, including adaptive equalization (AEQ), ASIL-B functional safety, and robust error monitoring diagnostics.

GMSL2 uses non-return to zero (NRZ) modulation which has a Nyquist frequency of half the transmission data rate. This translates to 3GHz for a 6Gbps link (or 1.5GHz for a 3Gbps link). Doubling the data rate while still using NRZ modulation translates to 6GHz for a 12Gbps link. However, there are disadvantages for using this higher frequency such as more insertion loss on the cable, connector, and PCB to reduce the total cable length of the application.

To avoid a higher frequency for double the data rate, GMSL3 leverages pulse-amplitude modulation 4 level (PAM4) to maintain the same Nyquist frequency as GMSL2. The lower operating frequency on the channel delivers many system benefits:

- GMSL2 and GMSL3 utilize the same clock link rate for schematic and layout reuse, operating on FR-4 PCBs.
- There is lower insertion loss on cables and connectors.
- Higher spectral efficiency by doubling the bandwidth and maintaining the same link rate.

The GMSL3 supports both 6Gbps with NRZ and 12Gbps with PAM4.

DESIGN CONSIDERATIONS

To demonstrate, consider the MAX96793 CSI-2 to GMSL3 serializer and the MAX96792A GMSL3 to CSI-2 deserializer. In general, the changes are minimal but need to be reviewed for each system application.

Pin-for-Pin Compatibility

GMSL devices between GMSL2 and GMSL3 generations are designed to be pin-for-pin compatible for design reuse. The serializer packages are 5mm x 5mm TQFN devices. Figure 1 details the pinouts of the MAX96717 and MAX96793:

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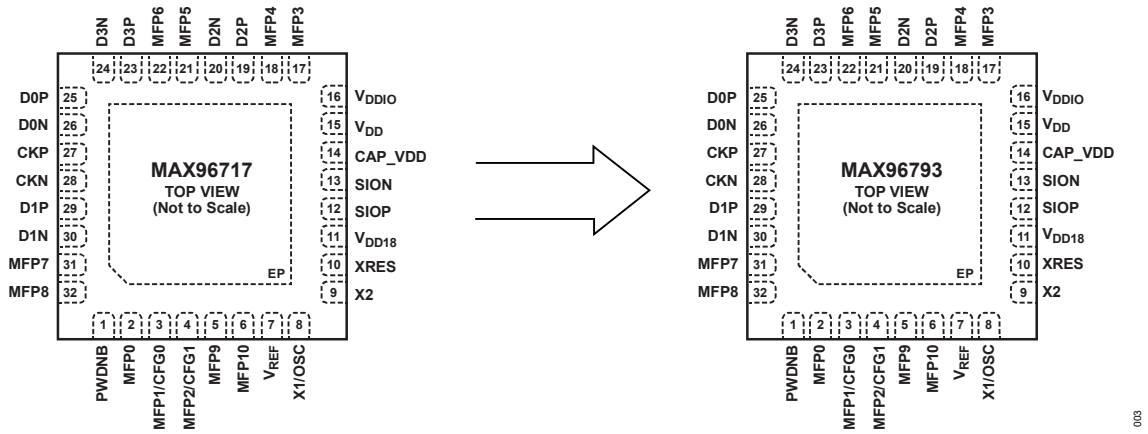

Figure 1. MAX96717 and MAX96793 Pinout Comparison

When using the reference clock over reverse (RoR) capability on these devices, connect a 20nF± 10% capacitor between the V_{REF} pin (pin 7) and ground. This connection is required for GMSL3 mode when using RoR and optional for GMSL2 mode to maintain optimal reverse link margin.

If RoR is not being used on GMSL3, this capacitor is not required.

The deserializer packages are 7mm x 7mm TQFN devices. Figure 2 details the pinouts of the MAX96716A and MAX96792A:

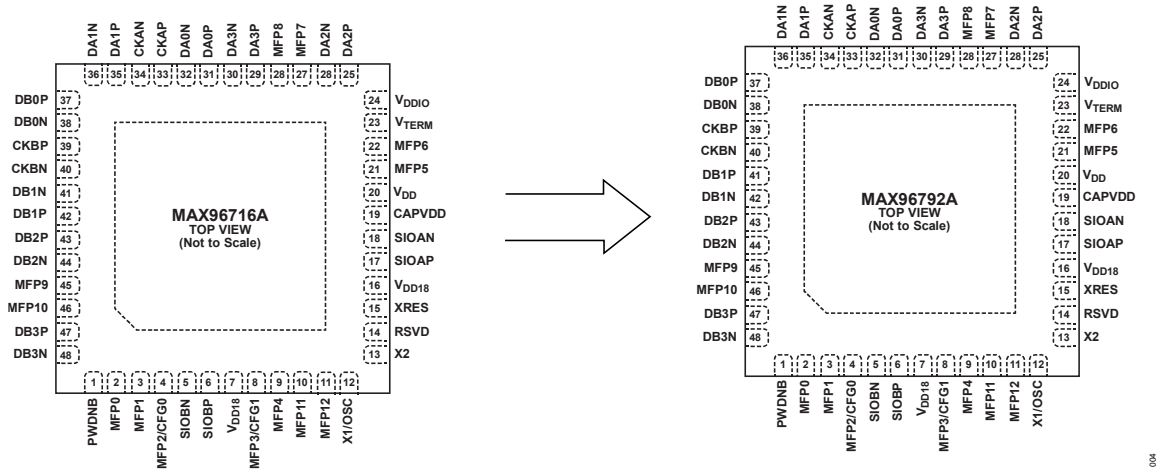

Figure 2. MAX96716A and MAX96792A Pinout Comparison

Power Consumption

Power consumption of these devices is characterized by using the physical layer interfaces to their full, operational capacity as detailed in the ***Configuration*** column of Table 1.

Table 1. Serializer Device Power Consumption Comparison

DEVICE	CONFIGURATION	I_{DD18}	I_{DD} (V_{DD} = 1.2V)	P_{TOTAL}
MAX96717	6Gbps Forward Link Rate (GMSL2 Mode) RGB888 Color Bar Pattern 4-lane CSI-2 DPHY	**46mA (25°C)** 53mA (105°C)	**98mA (25°C)** 232mA (105°C)	**~210mW (25°C)** ~393mW (105°C)

	input 1.3Gbps per lane			
MAX96793	12Gbps Forward Link Rate (GMSL3 Mode) RGB888 Color Bar Pattern 4-lane CSI-2 DPHY input 2.5Gbps per lane	**46mA (25°C)** 53mA (105°C)	**170mA (25°C)** 340mA (105°C)	**~301mW (25°C)** ~529mW (105°C)

Both devices utilize the same power supply rail voltages to simplify power-supply topology requirements. The V_{DD18} rail uses the same power for both of the MAX96717 and MAX96793 GMSL device families. The maximum current on V_{DD} core rail has only a slight current increase of approximately ~70mA (25°C) or ~110mA (105°C). Check the power-supply source to ensure there is enough margin on the rail to accommodate the current increase.

As previously mentioned, these devices are characterized by a configuration intended to use the physical layer interfaces to their fullest capacity, which translates to both GMSL inputs and both MIPI-CSI2 outputs for the deserializer. These devices can be used with a single GMSL input and/or a single MIPI-CSI2 output to reduce total power consumption.

Additionally, the camera deserializer devices have a MIPI-CSI2 supply rail V_{TERM} for the MIPI-CSI2 PHY.

Table 2. Deserializer Device Power Consumption Comparison

DEVICE	CONFIGURATION	I_{DD18}	I_{DD} (V_{DD} = 1.2V)	I_{TERM}	P_{TOTAL}
MAX96716A	6Gbps Forward Link Rate (GMSL2 Mode) 2x 6Gbps inputs 2x 4-Lane CSI-2 DPHY inputs 1.3Gbps per lane	**196mA (25°C)** 245mA (105°C)	**197mA (25°C)** 460mA (105°C)	**27mA (25°C)** 40mA (105°C)	**~654mW (25°C)** ~1095mW (105°C)
MAX96792A	12Gbps Forward Link Rate (GMSL3 Mode) 2x 12Gbps inputs 2x 4-Lane CSI-2 DPHY inputs 2.5Gbps per lane	**210mA (25°C)** 250mA (105°C)	**365mA (25°C)** 850mA (105°C)	**31mA (25°C)** 40mA (105°C)	**~898mW (25°C)** ~1596mW (105°C)

Both devices utilize the same power-supply rail voltages to simplify the power-supply topology requirements. The V_{DD18} rail uses approximately the same power for both of the MAX96716A and MAX96792A GMSL device families. The maximum current on V_{DD} core rail has a current increase of approximately ~160mA (25°C) or ~390mA (105°C). Check the power-supply source to ensure there is enough margin on the rail to accommodate the current increase.

Additionally, the quiescent current draw and the maximum power-supply noise tolerance is the same for both devices to maintain the same system requirements for both families.

Configuration Pin Settings

The configuration pins for these devices have only a few differences. It is important to confirm the configuration pin values from the device data sheet as these will determine how the devices will be configured at every bootup.

Figure 3 and Figure 4 show the details of the configuration pins, which are specific to the MAX96717 and MAX96793 for the sake of explanation. All configuration pin settings are device specific and detailed in their respective device data sheets.

Configuration 0 pin (CFG0) configures the communication channel interface between UART and I²C, the option to use RoR or crystal, and the device address.

Configuration 1 pin (CFG1) configures the cable type of STP or coax, the GMSL data rate, and the choice of tunnel or pixel mode. CFG1 has the minor differences for setting the GMSL data rate. The pixel mode data rates are the same between devices. The tunnel mode operation supports 6Gbps and 12Gbps for GMSL3 and 3Gbps and 6Gbps for GMSL2.

Table 11. CFG0 Input Map

CFG0 INPUT VOLTAGE SPECIFICATION (% OF V_{DDIO}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE c)		MAPPED CONFIGURATION (NOTE c)		
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	I2CSEL	RoR/ Xtal	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10k	I²C	RoR	0x80
16.9%	20.2%	23.6%	80.6k	20.5k			0x84
28.8%	32.1%	35.5%	68.1k	32.4k		Xtal	0x80
40.7%	44.0%	47.4%	56.2k	44.2k			0x84
52.6%	56.0%	59.3%	44.2k	56.2k	UART	RoR	0x84
64.5%	67.9%	71.2%	32.4k	68.1k			0x80
76.4%	79.8%	83.1%	20.5k	80.6k		Xtal	0x84
88.3%	100%	100%	10k	OPEN			0x80

Note a: Resistor-divider tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.

Note b: Other than the CFG0 input resistor-divider, any load on CFG0 must be ≥ 25 x (R1 + R2). Each resistor in the voltage-divider must be ≤ 100kΩ.

Note c: I2CSEL: I²C or UART interface for SDA_RX and SCL_TX.

Table 12. CFG1 Input Map

SPECIFICATION (% of V_{DDIO}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE)		MAPPED CONFIGURATION (NOTE c)		
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	COAX or TWISTED PAIR	DATA RATE (Gbps)	TUNNEL/PIXEL MODE
0%	0.0%	11.7%	OPEN	10k	STP	3	Tunnel
16.9%	20.2%	23.6%	80.6k	20.5k		6	
28.8%	32.1%	35.5%	68.1k	32.4k		3	Pixel
40.7%	44.0%	47.4%	56.2k	44.2k		6	
52.6%	56.0%	59.3%	44.2k	56.2k	COAX	3	Tunnel
64.5%	67.9%	71.2%	32.4k	68.1k		6	
76.4%	79.8%	83.1%	20.5k	80.6k		3	Pixel
88.3%	100%	100%	10k	OPEN		6	

Table 11. CFG0 Input Map

CFG0 INPUT VOLTAGE SPECIFICATION (% of VDDIO) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE c)		MAPPED CONFIGURATION (NOTE d)		
MIN	TYP	MAX	R1 [Ω]	R2 [Ω]	I2CSEL	RoR/ Xtal	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10k	I²C	RoR	0x80
16.9%	20.2%	23.6%	80.6k	20.5k			0x84
28.8%	32.1%	35.5%	68.1k	32.4k		Xtal	0x80
40.7%	44.0%	47.4%	56.2k	44.2k			0x84
52.6%	56.0%	59.3%	44.2k	56.2k	UART	RoR	0x84
64.5%	67.9%	71.2%	32.4k	68.1k			0x80
76.4%	79.8%	83.1%	20.5k	80.6k		Xtal	0x84
88.3%	100%	100%	10k	OPEN			0x80

Notes:

1. Resistor-divider tolerance, V_{DDIO} supply ripple and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.
2. Other than the CFG0 input resistor-divider, any load on CFG0 must be ≥ 25 x (R1 + R2).
3. Each resistor in the voltage divider must be ≤ 100kΩ.
4. I2CSEL: I2C or UART interface for SDA_RX and SCL_TX.

Table 12. CFG1 Input Map

SPECIFICATION (% of VDDIO) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE)		MAPPED CONFIGURATION (NOTE c)			
MIN	TYP	MAX	R1 [Ω]	R2 [Ω]	Coax or Twisted Pair	Data rate [Gbps]	Forward Channel Modulation	Tunnel/pixel mode
0%	0.0%	11.7%	OPEN	10k	STP	6	NRZ	Tunnel
16.9%	20.2%	23.6%	80.6k	20.5k		12	PAM4	
28.8%	32.1%	35.5%	68.1k	32.4k		3	NRZ	Pixel
40.7%	44.0%	47.4%	56.2k	44.2k		6		
52.6%	56.0%	59.3%	44.2k	56.2k	COAX	6	NRZ	Tunnel
64.5%	67.9%	71.2%	32.4k	68.1k		12	PAM4	
76.4%	79.8%	83.1%	20.5k	80.6k		3	NRZ	Pixel
88.3%	100%	100%	10k	OPEN		6		

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Figure 3. MAX96717 (left) and MAX96793 (right) Configuration Pin Comparison

Table 12. CFG0 Input Map

CFG0 INPUT VOLTAGE SPECIFICATION (% of V_{DDIO}) (Notes a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION (Notes d, e)	
MIN	TYP	MAX	R1 [Ω]	R2 [Ω]	I2CSEL	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10k	I²C	0x50
16.9%	20.2%	23.6%	80.6k	20.5k		0x54
28.8%	31.2%	35.5%	68.1k	32.4k		0x98
40.7%	44.0%	47.4%	56.2k	44.2k		0xD4
52.6%	56.0%	59.3%	44.2k	56.2k	UART	0xD4
64.5%	67.9%	71.2%	32.4k	68.1k		0x98
76.4%	79.8%	83.1%	20.5k	80.6k		0x54
88.3%	100%	100%	10k	OPEN		0x50

Notes:

a. Resistor-divider tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.
b. Other than the CFG0 input resistor-divider, any load on CFG0 must be ≥ 25 x (R1 + R2).
c. Each resistor in the voltage divider must be ≤ 100kΩ.
d. I2CSEL: I²C or UART interface for SDA_RX and SCL_TX.
e. When this address is selected, both serial inputs are automatically enabled. A single serial input can be programmed after power-up, if desired.

Table 13. CFG1 Input Map

SPECIFICATION (% of V_{DDIO}) (Notes a,b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION		
MIN	TYP	MAX	R1 [Ω]	R2 [Ω]	COAX OR TWISTED PAIR	DATA RATE [Gbps]	TUNNEL/ PIXEL MODE
0.0%	0.0%	11.7%	OPEN	10k	STP	3	Tunnel
16.9%	20.2%	23.6%	80.6k	20.5k		6	
28.8%	32.1%	35.5%	68.1k	32.4k		3	Pixel
40.7%	44.0%	47.4%	56.2k	44.2k		6	
52.6%	56.0%	59.3%	44.2k	56.2k	COAX	3	Tunnel
64.5%	67.95%	71.2%	32.4k	68.1k		6	
76.4%	79.8%	83.1%	20.5k	80.6k		3	Pixel
88.3%	100%	100%	10k	OPEN		6	

Table 12. CFG0 Input Map

CFG0 INPUT VOLTAGE SPECIFICATION (Notes a, b) (% of V_{DDIO})			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION (Note d, e)	
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	I2CSEL	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10k	I²C	0x50
16.9%	20.2%	23.6%	80.6k	20.5k		0x54
28.8%	31.2%	35.5%	68.1k	32.4k		0x98
40.7%	44.0%	47.4%	56.2k	44.2k		0xD4
52.6%	56.0%	59.3%	44.2k	56.2k	UART	0xD4
64.5%	67.9%	71.2%	32.4k	68.1k		0x98
76.4%	79.8%	83.1%	20.5k	80.6k		0x54
88.3%	100%	100%	10k	OPEN		0x50

Notes:

a. Resistor divider tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.
b. Other than the CFG0 input resistor divider, any load on CFG0 must be ≥ 25 x (R1 + R2).
c. Each resistor in the voltage divider must be ≤ 100kΩ.
d. I2CSEL: I²C or UART interface for SDA_RX and SCL_TX.
e. When this address is selected, both serial inputs are automatically enabled. A single serial input can be programmed after power-up, if desired.

Table 13. CFG1 Input Map

SPECIFICATION (Notes a, b) (% of V_{DDIO})			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION			
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	COAX OR TWISTED PAIR	DATA RATE [Gbps]	FORWARD CHANNEL MODULATION	TUNNEL/ PIXEL MODE
0.0%	0.0%	11.7%	OPEN	10k	STP	6	NRZ	Tunnel
16.9%	20.2%	23.6%	80.6k	20.5k		12	PAM4	
28.8%	32.1%	35.5%	68.1k	32.4k		3		Pixel
40.7%	44.0%	47.4%	56.2k	44.2k		6	NRZ	
52.6%	56.0%	59.3%	44.2k	56.2k	COAX	6		Tunnel
64.5%	67.95%	71.2%	32.4k	68.1k		12	PAM4	
76.4%	79.8%	83.1%	20.5k	80.6k		3	NRZ	Pixel
88.3%	100%	100%	10k	OPEN		6		

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Figure 4. MAX96716A (left) and MAX96792A (right) Configuration Pin Comparison

PAM4 Modulation Scheme

PAM4 is an existing modulation scheme that GMSL leverages for rigorous automotive environments. Where NRZ uses two voltage levels to represent a 1-bit symbol, PAM4 uses four voltage levels to represent a 2-bit symbol to allow GMSL3 to operate at the same baud rate as GMSL2 and double the bit rate of data transmitted.

Doubling the data rate, however, is not without consequences; the tradeoff is that PAM4 has a smaller eye opening that is approximately 1/3 of the NRZ eye opening.

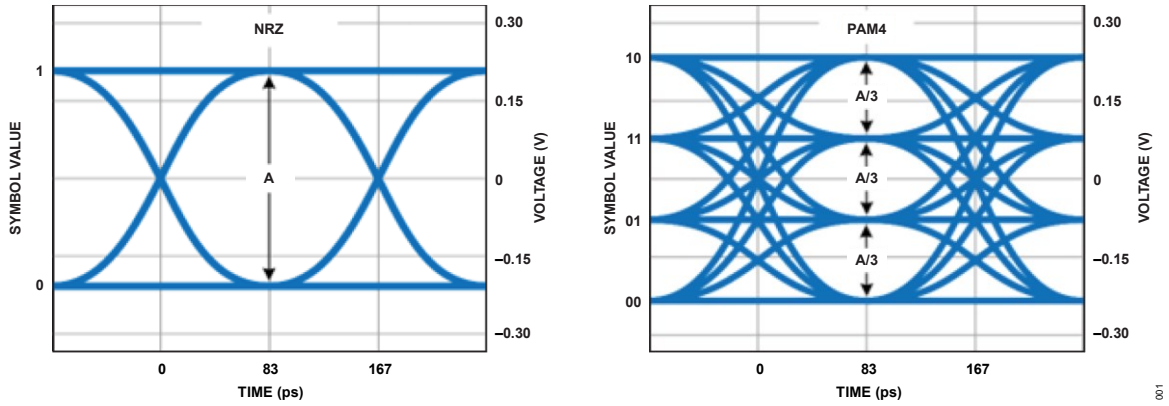

Figure 5. Modulation Comparison of NRZ (left) and PAM4 (right)

In Figure 5, 'A' is defined as the NRZ eye opening, which means that if NRZ transmits 1 bit per period (1/T) with an SNR of A, then PAM4 transmits 2 bits per period (2/T) with an SNR of A/3.

Forward Error Correction

To overcome this noise sensitivity inherent with PAM4, GMSL3 includes forward-error correction (FEC) to add data redundancy and error correction capabilities to the link. FEC can significantly reduce the SNR requirement and helps decrease the bit error rate (BER) of the link to essentially one bit error for the lifetime of the GMSL link.

GMSL FEC utilizes Reed-Solomon encoding, which is found in CDs, QR codes, and even the Voyager spacecraft **[1]**. Additionally, this FEC information can be monitored in real time with registers or conveniently in the GMSL GUI.

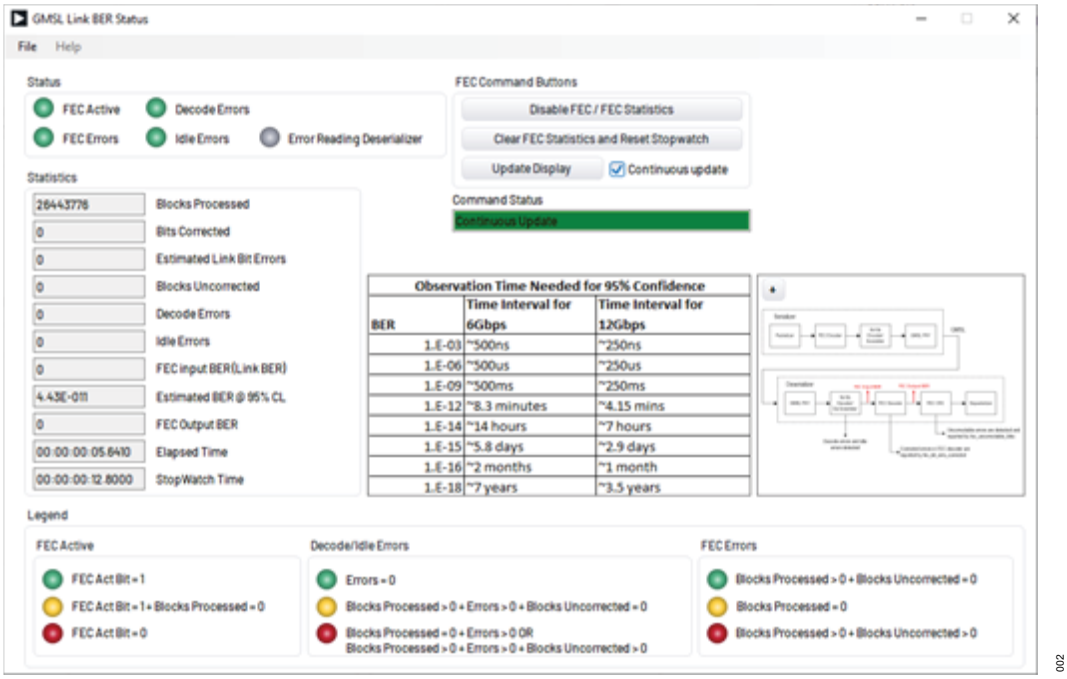

Figure 6. GMSL Link BER Status Window from the GMSL GUI

Since FEC is mandatory for GMSL3 operation, the bandwidth impact needs to be factored in when confirming a use case has sufficient bandwidth. Using FEC consumes an additional 6.67% (128/120) on the GMSL link for the added BER robustness. The GMSL bandwidth calculator in the GMSL GUI includes this overhead in the calculation. This overhead translates to approximately ~9.7Gbps of useable bandwidth on the GMSL3 link.

Table 7. Forward- and Reverse-Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video (Forward Path Only)	Bandwidth = PCLK x (bpp + 1 + video_pixel_CRC) x 10/9 x 2048/2047 x 128/120* Pixel mode PCLK Calculations: PCLK = MIPI data rate/bpp PCLK = MIPI data rate/(2 x bpp) for double pixel mode PCLK = MIPI data rate/(3 x bpp) for triple pixel mode Tunnel mode PCLK calculations: PCLK = MIPI data rate/24 Bandwidth Notes: 1. The link bandwidth calculation uses the bpp value of the video pipe with highest bpp value of the transmitted datatype(s) (Pixel mode only). 2. Maximum bandwidth is limited by pixel clock rate PCLK. 3. video_pixel_CRC=0.5 (when video pixel CRC is enabled) PCLK Notes: 1. The PCLK calculation uses datatype with the lowest bpp value (Pixel mode only). 2. Maximum PCLK is 300MHz for 3Gbps link rate 3. Maximum PCLK is 600MHz for 6Gbps link rate 4. MIPI data rate includes horizontal and vertical blanking times (*only applies when GMSL FEC is enabled)
I²C	13 to 40 x I²C clock rate
UART	6 x UART bit rate
SPI	1.7 to 3.1 x SPI rate, depending on SPI byte length
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Note: Bandwidth utilization for all video and control-channel communication in the forward direction increases by 6.7% when forward-error correction (FEC) is enabled.

Figure 7. FEC Impact on Useable Bandwidth of GMSL3

Error Reporting

When using FEC on the GMSL3 link, a different error monitoring ideology is required based on the system monitoring requirements. FEC allows for detecting and correcting errors that may occur on the link so it is possible to have FEC

correctable bits since the devices report the corrections. FEC uncorrectable bits are not allowed, which indicates that the GMSL3 device is unable to correct an error that occurred on the link.

As a result, error monitoring needs to be adjusted depending on what is deemed an error. For GMSL2 mode, decode and idle errors are used to report errors occurring on link. For GMSL3 mode, FEC uncorrectable errors are used to report errors on the link; FEC corrected bits are also reported.

By default, the FEC error flag checks correctable and uncorrectable bits and reports to ERRB pin. The FEC threshold for correctable bits must be adjusted to the system requirements. Error monitoring changes are detailed in the software differences section.

Channel Specification

A significant change between GMSL2 and GMSL3 is the GMSL channel specification. Do not assume that a compliant GMSL2 system is compatible with the GMSL3 channel specification due to the stricter budget. Refer to the latest GMSL2 channel specification and GMSL3 channel specification available on analog.com.

It is important to reevaluate PCB layouts and cabling needs when reusing designs.

GMSL3 (12Gbps) and GMSL2 (6Gbps) both operate with a fundamental 3GHz link frequency.

GMSL3 insertion loss requirements are additionally specified with both a long channel (high loss) and short channel (low loss). A short channel has a tighter insertion loss (IL), but a relaxed return loss (RL).

GMSL3 return loss requirements are additionally specified with both a long channel (high loss) and a short channel (low loss). A short channel has a relaxed RL, but a tighter IL.

The S-parameter data must be filtered before comparing it to the GMSL3 IL and RL limits. A 100MHz filter is applied to the S-parameters across the full range. Apply unfiltered data from the lowest captured frequency up to 50MHz. Beyond 50MHz, use filtered data to compare to the limit.

Register Settings Difference

There are two main software differences between these devices: operating in GMSL3 mode and error monitoring.

For GMSL3 mode, all the following changes detailed in Table 3 and Table 4 are handled through the CFG pins. These pins correctly configure the device's transmit and receive speed along with the PAM4 modulation. Table 3 and Table 4 identify the registers in case the software is programming or overriding the CFG pins, which is not typically recommended.

Note: If using CFG pins to configure the GMSL mode, the following changes shown in Table 3 and Table 4 are not required.

The programming procedure needs to be performed in a specific order. Start with the remote device, then follow with the local device. Remote and local terminology refer to the location of the I^2C controller. Programming the local device prevents communication to the remote device. For this example, the MAX96793 is the remote device and the MAX96792A (which is connected to the I^2C controller) is the local device.

Table 3. Programming Procedures from 6Gbps GMSL2 to 12Gbps GMSL3

STEP	LOCATION	DEVICE	DESCRIPTION	REGISTER	VALUE
1	Remote	MAX96793	Change Tx rate to 12Gbps	0x0001	REG1[3:2] = 0b11

2	Remote	MAX96793	Enable FEC	0x0028	TX0[1] = 0b1
3	Remote	MAX96793	Disable GMSL2 mode and enable GMSL3 mode	0x0006	REG6[7] = 0b0
4	Local	MAX96792A	Hold the GMSL link in RESET	0x0010	CTRL0[6] = 0b1
5	Local	MAX96792A	Change Rx rate to 12Gbps	0x0001	REG1[1:0] = 0b11
6	Local	MAX96792A	Enable FEC	0x0028	TX0[1] = 0b1
7	Local	MAX96792A	Disable GMSL2 mode and enable GMSL3 mode	0x0004	REG4[7:6] = 0b11*
8	Local	MAX96792A	Release the GMSL link from RESET	0x0010	CTRL0[6] = 0b0

**This sets both links to GMSL3. Each link can be configured individually.*

Table 4. Programming Procedures from 12Gbps GMSL3 to 6Gbps GMSL2

STEP	LOCATION	DEVICE	DESCRIPTION	REGISTER	VALUE
1	Remote	MAX96793	Change Tx rate to 6Gbps	0x0001	REG1[3:2] = 0b10
2	Remote	MAX96793	Disable FEC	0x0028	TX0[1] = 0b0
3	Remote	MAX96793	Enable GMSL2 mode and disable GMSL3 mode	0x0006	REG6[7] = 0b0
4	Local	MAX96792A	Hold the GMSL link in RESET	0x0010	CTRL0[6] = 0b1
5	Local	MAX96792A	Change Rx rate to 6Gbps	0x0001	REG1[1:0] = 0b10
6	Local	MAX96792A	Disable FEC	0x0028	TX0[1] = 0b0
7	Local	MAX96792A	Enable GMSL2 mode and disable GMSL3 mode	0x0004	REG4[7:6] = 0b00*
8	Local	MAX96792A	Release the GMSL link from RESET	0x0010	CTRL0[6] = 0b0

**This sets both links to GMSL3. Each link can be configured individually.*

As mentioned in the *Error Reporting* section, the error monitoring ideology does need to change depending on the FEC reporting.

Table 5. GMSL2 Error Reporting without FEC Enabled

	MAX96793	MAX96792A

BIT NAME	REGISTER	VALUE	REGISTER	VALUE
DEC_ERR_OEN_A	0x001A	INTR2[0] = 0b1	0x001A	INTR2[0] = 0b1
DEC_ERR_OEN_B	—	—	0x001A	INTR2[1] = 0b1
IDLE_ERR_OEN	0x001A	INTR2[2] = 0b1	0x001A	INTR2[2] = 0b1
IDLE_ERR_OEN_B	—	—	0x5010	INTR10[6] = 0b1
FEC_RX_ERR_OEN	—	—	0x001C	INTR4[5] = 0b0*
FEC_RX_ERR_OEN_B	—	—	0x5010	INTR10[5] = 0b0*

**Each link can be configured individually.*

Table 6. GMSL3 Error Reporting with FEC Enabled

	MAX96793		MAX96792A	
BIT NAME	**REGISTER**	**VALUE**	**REGISTER**	**VALUE**
DEC_ERR_OEN_A	0x001A	INTR2[0] = 0b0	0x001A	INTR2[0] = 0b0
DEC_ERR_OEN_B	—	—	0x001A	INTR2[1] = 0b0
IDLE_ERR_OEN	0x001A	INTR2[2] = 0b0	0x001A	INTR2[2] = 0b0
IDLE_ERR_OEN_B	—	—	0x5010	INTR10[6] = 0b0
FEC_RX_ERR_OEN	—	—	0x001C	INTR4[5] = 0b1*
FEC_RX_ERR_OEN_B	—	—	0x5010	INTR10[5] = 0b1*

**Each link can be configured individually.*

With FEC enabled, the FEC statistics can be configured individually for the applications requirements. There is an abundance of registers for the MAX96792A, which starts at register block address 0x2000 to read the statistics and set error thresholds for both links.

For example, your application may allow for a certain number of correctable bit errors before raising alarm so set the CORRECTED_THRESHOLD_0/1/2/3 to the permitted number of corrected bits. Uncorrectable bit errors are more concerning and indicate a greater problem in the system.

The breadth of statistics allows for a comprehensive GMSL link state of health.

CONCLUSION

The GMSL2 and GMSL3 device families are designed to grow with designs and the details outlined show the changes to consider when upgrading a system. In general, GMSL2 and GMSL3 devices remain as consistent as possible to alleviate the design burden when upgrading. As two specific device upgrades are detailed in this article, it is mandatory to review the documentation of any additional GMSL2 and GMSL3 devices for the design. However, GMSL bandwidth calculations and GMSL channel specifications remain consistent for all GMSL devices.

REFERENCES

[1] Canterbury, “QR codes - Coding - Error control - Computer Science Field Guide,” *Csfieldguide.org.nz*, 2024. https://www.csfieldguide.org.nz/en/chapters/coding-error-control/qr-codes.